REMARKS

Claims 1-19 are currently pending in the subject application and are presently under consideration. A version of all pending claims is found at pages 2-6. Applicants' representative notes with appreciation the indication that the objection to claim 5 for minor informalities, and the rejection of claim 3 under 35 U.S.C. §112, second paragraph, have been withdrawn by the Examiner. Favorable consideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claims 1-19 Under 35 U.S.C. §103(a)

Claims 1-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Schmidt *et al.* (US 5,212,631), in view of Sharma *et al.* (US 6,085,263). It is respectfully requested that this rejection should be withdrawn for at least the following reason. Schmidt *et al.* and Sharma *et al.*, either alone or in combination, fail to teach or suggest all the limitations set forth in the subject claims.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) ***must teach or suggest all the claim limitations.*** *See* MPEP §706.02(j). The *teaching or suggestion to make the claimed combination* and the reasonable expectation of success *must be found in the prior art and not based on the Applicant's disclosure. See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

The invention as claimed relates to a system and method for I/O forcing using an I/O processor having cache memory, wherein a processor and an I/O processor are operatively coupled to shared memory. In particular, the present invention as recited in independent claim 1 sets forth an I/O processor operatively coupled to a cache memory wherein a portion of the forced I/O values are stored in the shared memory, the I/O

processor storing input values in shared memory based at least in part upon ***forced I/O values stored in the cache memory***, and further the I/O processor determines output values based at least in part upon ***the forced I/O values stored in the cache memory***. Moreover, independent claims 6, 9, 10 and 17 recite similar limitations. Schmidt *et al.* is silent regarding these limitations, and Sharma *et al.* fails to rectify the deficiencies presented by Schmidt *et al.*

As the Examiner acknowledges, Schmidt *et al.* alone fails to teach or suggest all the limitations recited in the subject claims, in particular, an I/O processor operatively coupled to a cache memory storing at least a portion of the forced I/O values stored in the shared memory. Applicants' representative asserts that Schmidt *el al.*, in addition to the deficiency identified by the Examiner, also fails to disclose ***forced I/O values stored in the cache memory***. In order to rectify the acknowledged deficiency the Examiner relies upon Sharma *et al.* to make up that which Schmidt *et al.* fails to teach. However, the Examiner fails to address the deficiency noted by applicants' representative and thus it appears that both Schmidt *et al.* and Sharma *et al.* fail to teach or suggest the noted limitation.

Sharma *et al.* discloses an I/O processor (IOP) for delivering high I/O performance while maintaining inter-reference ordering among memory reference operations issued by an I/O device as specified by a consistency model in a shared memory multiprocessor system. Specifically, Sharma *et al.* discloses an IOP that comprises:

> ... a plurality of input request queues that interface an I/O bus to receive memory reference operations issued by the I/O device ... [the] head of each input queue is coupled to a prefetch controller ... [and] the prefetch controller examines the address of each memory reference operation at the queue head and compares it with the addresses stored in the cache entries. *See*, col. 14, lines 9-23.

It is apparent that Sharma *et al.*, rather than storing ***a portion of the forced I/O values in the cache memory***, stores prefetched transient input and output data into cache without any ordering constraints to ensure maximum throughput of data through the I/O

processor. (*See*, col. 13, lines 61-62). In contrast, applicants' claimed invention segregates extremely dynamic input and output data generated by I/O devices from relatively static I/O force data and configuration data and places only the I/O force data and configuration data into the cache, leaving the dynamic input and output data to reside in shared memory. Sharma *et al.* is indiscriminate regarding the type of data that is stored in cache, and in particular is directed towards storing in cache what the claimed invention deems to be non-cacheable data, *e.g.*, input and output data received and directed to an I/O device. The invention as claimed therefore, is distinguishable from both Sharma *et al.* and Schmidt *et al.* on this ground. Further, since the type of data stored in the cache is relatively static, *e.g.*, I/O force data, the invention as claimed obviates both the necessity of the prefetch controller disclosed in Sharma *et al.*, and the necessity to expedite the fetching of data into cache memory, and thus the motivation to combine Schmidt *et al.* and Sharma *et al.* is lacking.

In view of at least the foregoing, it is respectfully requested that the rejection of independent claims 1, 6, 9, 10 and 17 (and claims that depend therefrom) should be withdrawn.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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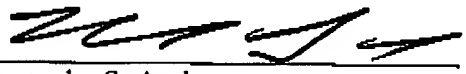

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